Claims

[c1] A method of forming a SiGe layer on a substrate, the method comprising the steps of:
depositing a first layer of one of Si and Ge in a first depositing step;
depositing a second layer of the other of Si and Ge on the first layer in a second depositing step; and
repeating said first depositing step and said second depositing step so as to form a combined SiGe layer having a plurality of Si layers and a plurality of Ge layers,
wherein respective thicknesses of the Si layers and Ge layers are in accordance with a desired composition ratio of the combined SiGe layer, and
the combined SiGe layer is characterized as a digital alloy of Si and Ge having a thermal conductivity greater than that of a random alloy of Si and Ge.

[c2] A method according to claim 1, wherein each of the Ge layers has a thickness of about 10 Å.

[c3] A method according to claim 1, further comprising the step of:
depositing a Si layer on the combined SiGe layer,
wherein the combined SiGe layer is further characterized

as a relaxed SiGe layer, and said Si layer is a strained Si layer.

[c4] A method according to claim 1, wherein the substrate comprises a silicon-on-insulator (SOI) structure.

[c5] A method according to claim 1, wherein the substrate comprises a SiGe-on-insulator (SGOI) structure.

[c6] A method according to claim 1, wherein the substrate has an upper layer, and further comprising the step of polishing said upper layer to reduce the thickness thereof, before said first depositing step.

[c7] A method according to claim 1, wherein at least one of the first layer and the second layer consists essentially of a single isotope.

[c8] A method of fabricating a semiconductor device, comprising the steps of:
forming a layer of a digital alloy of SiGe on a substrate; and
forming a Si layer on the digital alloy of SiGe,
wherein the digital alloy of SiGe has a thermal conductivity greater than that of a random alloy of Si and Ge.

[c9] A method according to claim 8, wherein the digital alloy layer is characterized as a relaxed SiGe layer, and said Si

layer is a strained Si layer.

[c10] A method according to claim 8, wherein the digital alloy layer includes a plurality of alternating sublayers of Si and Ge.

[c11] A method according to claim 10, wherein the sublayers are formed with thicknesses in accordance with a desired composition ratio of the digital alloy of SiGe.

[c12] A method according to claim 10, wherein each of the sublayers consists essentially of a single isotope.

[c13] A semiconductor device comprising:
a layer of a digital alloy of SiGe on a substrate; and
a Si layer on the digital alloy of SiGe,
wherein the digital alloy of SiGe has a thermal conductivity greater than that of a random alloy of Si and Ge.

[c14] A device according to claim 13, wherein the digital alloy layer is characterized as a relaxed SiGe layer, and said Si layer is a strained Si layer.

[c15] A device according to claim 13, wherein the digital alloy layer includes a plurality of alternating sublayers of Si and Ge.

[c16] A device according to claim 15, wherein the sublayers are formed with thicknesses in accordance with a desired

composition ratio of the digital alloy of SiGe.

[c17] A device according to claim 15, wherein each of the sub-layers consists essentially of a single isotope.

[c18] A device according to claim 15, wherein each of the Ge layers has a thickness of about 10 Å.

[c19] A device according to claim 15, wherein a sublayer of Si is disposed on the substrate.

[c20] A device according to claim 13, wherein the substrate is a silicon-on-insulator (SOI) structure.